EE 542
Digital Systems Verification and Testing
Fall 2005

- **Instructor**: Ilker Hamzaoglu  
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  MDBF 1037

- **Lectures**:  
  M 11:40 am - 12:30 pm FENS L061  
  M 1:40 pm - 3:30 pm FENS L062

- **Web Site**: [http://people.sabanciuniv.edu/~hamzaoglu/ee542/ee542.htm](http://people.sabanciuniv.edu/~hamzaoglu/ee542/ee542.htm)
Course Description

This course introduces the problems of design verification and testing.

It then covers the digital systems testing process, various fault models, automatic test pattern generation (ATPG), fault simulation, memory test, design for testability, built-in self-test, SoC test structures.

After that, the course covers the design verification process, simulation-based verification, emulation-based verification and formal verification.

Finally, it covers ATPG-based verification techniques.

In this course, students will also gain practical testing and verification experience by using several CAD tools from Synopsys (DFT Compiler, TetraMax ATPG, Formality) and Mentor Graphics (Modelsim), and by writing a small scale CAD software implementing a testing algorithm.
### Course Motivation

#### 1H05 Top 10 Worldwide Semiconductor Supplier Ranking ($M)

<table>
<thead>
<tr>
<th>Rank</th>
<th>Company</th>
<th>Headquarters</th>
<th>1Q05 Sales ($M)</th>
<th>2005 Sales ($M)</th>
<th>1H05 Sales ($M)</th>
<th>2Q05/1Q05 % Change</th>
<th>2004 Sales ($M)</th>
<th>1H05 as a % of Total '04 Sales</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Intel</td>
<td>U.S.</td>
<td>8,520</td>
<td>8,335</td>
<td>16,855</td>
<td>-2%</td>
<td>30,900</td>
<td>55%</td>
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<tr>
<td>2</td>
<td>Samsung</td>
<td>South Korea</td>
<td>4,361</td>
<td>4,133</td>
<td>8,494</td>
<td>-5%</td>
<td>15,830</td>
<td>54%</td>
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<tr>
<td>3</td>
<td>Texas Instruments</td>
<td>U.S.</td>
<td>2,597</td>
<td>2,765</td>
<td>5,362</td>
<td>6%</td>
<td>10,700</td>
<td>50%</td>
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<td>4</td>
<td>Renesas</td>
<td>Japan</td>
<td>2,450</td>
<td>2,400</td>
<td>4,850</td>
<td>-2%</td>
<td>9,000</td>
<td>54%</td>
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<tr>
<td>5</td>
<td>Toshiba</td>
<td>Japan</td>
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<td>2,061</td>
<td>4,336</td>
<td>-9%</td>
<td>8,531</td>
<td>51%</td>
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<td>6</td>
<td>STMicroelectronics</td>
<td>Europe</td>
<td>2,081</td>
<td>2,161</td>
<td>4,242</td>
<td>4%</td>
<td>8,760</td>
<td>48%</td>
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<tr>
<td>7</td>
<td>Infineon</td>
<td>Europe</td>
<td>2,113</td>
<td>2,023</td>
<td>4,136</td>
<td>-4%</td>
<td>9,180</td>
<td>45%</td>
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<tr>
<td>8</td>
<td>TSMC</td>
<td>Taiwan</td>
<td>1,765</td>
<td>1,861</td>
<td>3,626</td>
<td>5%</td>
<td>7,648</td>
<td>47%</td>
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<tr>
<td>9</td>
<td>Freescale</td>
<td>U.S.</td>
<td>1,427</td>
<td>1,460</td>
<td>2,887</td>
<td>2%</td>
<td>5,519</td>
<td>52%</td>
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<tr>
<td>10</td>
<td>NEC</td>
<td>Japan</td>
<td>1,519</td>
<td>1,305</td>
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<td>6,469</td>
<td>44%</td>
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<td><strong>Total Top 10</strong></td>
<td></td>
<td><strong>29,108</strong></td>
<td><strong>28,504</strong></td>
<td><strong>57,612</strong></td>
<td>-2%</td>
<td><strong>112,537</strong></td>
<td>51%</td>
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<td>11</td>
<td>Philips</td>
<td>Europe</td>
<td>1,377</td>
<td>1,420</td>
<td>2,797</td>
<td>3%</td>
<td>5,692</td>
<td>49%</td>
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<tr>
<td>12</td>
<td>Sony</td>
<td>Japan</td>
<td>1,414</td>
<td>1,209</td>
<td>2,623</td>
<td>-14%</td>
<td>5,070</td>
<td>52%</td>
</tr>
</tbody>
</table>

Source: Company Reports, IC Insights
References

• **Lecture Slides**
  – Instructor’s slides, Textbook slide set, UIUC ECE443 lecture slides by E. M. Rudnick

• **Textbook:** Essentials of Electronic Testing

• Various papers and presentations from the literature
Recommended Books

• Digital Systems Testing and Testable Design
  Miron Abramovici, Melvin A. Breuer, Arthur D. Friedman, IEEE, 1994

• Design-For-Test for Digital ICs and Embedded Core Systems
  Alfred Crouch, Pearson Education, 1999

• Functional Verification of HDL Models

• System-on-a-Chip Verification: Methodology and Techniques
  Prakash Rashinkar, Peter Paterson, Leena Singh,

• Introduction to Formal Hardware Verification
  Thomas Kropf, Springer-Verlag, 1999
Tentative Schedule

- Digital Systems Verification vs Testing
- Testing
  - Test Equipment and Testing Process
  - Fault Modeling
  - Automatic Test Pattern Generation (ATPG)
  - Fault Simulation
  - Test Set Compaction
  - Delay Test
  - Memory Test
  - Design for Testability (DFT)
  - Scan Design
  - Built-in Self-Test (BIST)
  - Boundary Scan Standard
  - System-on-a-Chip (SoC) Test Structures
Tentative Schedule

• Verification
  – Design Verification Process
  – Simulation-based Verification
  – Emulation-based Verification
  – Formal Verification
  – Equivalence Checking
  – Binary Decision Diagrams (BDD)

• ATPG-based Verification Techniques
  – Design Error Detection
  – Equivalence Checking
  – Timing Verification
Grading

• Lab #1 (25%)
  – Develop a small scale CAD software implementing a testing algorithm

• Lab #2 (25%)
  – Use a commercially available verification or testing CAD tool on a design

• Paper Presentation (25%)
  – Study a recently published paper in the literature about verification or testing and present it in the class

• Final Exam (25%)