EL401 VLSI System Design I
Fall 2014

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Course Structure

• EL 401  VLSI Systems Design I  
  M 3:40 pm - 5:30 pm FENS L058  
  R 1:40 pm - 2:30 pm FENS L067

• EL 401L  VLSI Systems Design I Lab  
  R 11:40 am - 12:30 pm FENS G025
Description

This course discusses fundamentals of digital CMOS VLSI design, and it covers full-custom and standard cell based digital VLSI circuit design. Students will learn the design flow for both design styles and they will become familiar with the issues involved in the individual design steps. They will also gain practical design experience by using several CAD tools (Synopsys Design Compiler, Mentor Graphics Modelsim, Cadence Virtuoso and Cadence SoC Encounter) to design, implement and verify a VLSI circuit.
References

- **Lecture Slides**
- **Textbooks**
  - Static Timing Analysis for Nanometer Designs: A Practical Approach, Jayaram Bhasker and Rakesh Chadha, Springer
  - Application-Specific Integrated Circuits, Michael J. S. Smith, Addison Wesley
- **Recommended Books**
  - CMOS VLSI Design, A Circuits and Systems Perspective, Neil Weste and David Harris, Addison-Wesley, 3rd edition
  - Timing Verification of ASICs, Farzad Nekoogar, Prentice Hall
  - Closing the Gap between ASIC & Custom, David Chinnery, Kurt Keutzer, Kluwer Academic Publishers
Tentative Schedule

• Introduction
• VLSI Design Styles
• CMOS Fabrication
• Standard Cell based VLSI Design
  – Standard Cell Libraries
  – Logic Synthesis, Synopsys Design Compiler
  – Floorplanning, Partitioning
  – Power Distribution
  – I/O Pads and Packaging
  – Placement and Routing
  – Dynamic and Static Timing Verification
Tentative Schedule

• Full-Custom CMOS VLSI Design
  – Capacitance, Resistance and Delay Estimation
  – CMOS Circuit and Layout Design
  – Arithmetic Circuits Design
    (Adders, Shifters, Multipliers)

• Low Power CMOS VLSI Design

• Timing in VLSI Circuits
  (Clock Generation and Distribution, Synchronization)

• Semiconductor Memories
Grading

• Attendance 5%
• Labs 35%  (Lab1 15%, Lab2 5%, Lab3 15%)
• Midterm 30%
• Final 30%

• Students can work in groups of two for the lab assignments. The lab assignments will be done using Sun Workstations in the VLSI Design Lab.

• Cheating in labs and exams is not allowed. It will be strongly penalized.