

Ilker Hamzaoglu

Electronics Engineering
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EDUCATION

PhD, 9/1999, Computer Science, University of Illinois at Urbana-Champaign, USA
Thesis: Test Pattern Generation and Test Application Time Reduction Algorithms for VLSI Circuits
GPA: 4 (over 4)

MS, 7/1993, Computer Engineering, Bogazici University, Istanbul, Turkey
Thesis: Machine Translation from Turkish to Other Turkic Languages
GPA: 4 (over 4), Rank: 1st in the Department

BS, 7/1991, Computer Engineering, Bogazici University, Istanbul, Turkey
GPA: 3.66 (over 4), High Honor Student, Rank: 1st in the Department

WORK EXPERIENCE

9/2003 - present, Assistant Professor
Electronics Engineering, Faculty of Engineering & Natural Sciences, Sabanci University, Istanbul, Turkey

12/2002 - 8/2003, Principle Staff Engineer (E11)
8/1999 - 11/2002, Senior Staff Engineer (E10)
Multimedia Architecture Lab, Motorola Labs, Schaumburg, IL, USA

Summer 1998 and Summer 1999, Visiting Lecturer
Department of Computer Science, University of Illinois at Urbana-Champaign, IL, USA

6/1996 - 9/1996, Staff Research Assistant
Computational Science Methods Group, X Division, Los Alamos National Laboratory, NM, USA

1/1994 - 7/1999, Teaching and Research Assistant
Computer Science and Electrical and Computer Engineering Departments, University of Illinois at Urbana-Champaign, IL, USA

9/1991 - 7/1993, Teaching and Research Assistant
Department of Computer Engineering, Bogazici University, Istanbul, Turkey

RESEARCH INTERESTS

Digital System-on-Chip ASIC and FPGA Design, Low Power Digital VLSI Design, Digital Video Processing and Compression, Computer-Aided Testing of Digital Systems, Parallel Processing

RESEARCH EXPERIENCE

9/2003 - present, Assistant Professor
Electronics Engineering, Sabanci University, Istanbul, Turkey

I founded SoC Design & Test Lab (<http://fens.sabanciuniv.edu/soclab>) at Sabanci University.

Current Projects

Project: Low Power Motion Estimation Hardware Design for Video Compression and Frame Rate Conversion

Supported by TUBITAK(The Scientific and Technological Research Council of Turkey), EEEAG 108E239

Duration: February 2009 - January 2011

Budget: \$100,000

Contribution: I'm directing this research project and 2 graduate students are working in this project under my supervision.

Project: Low Complexity Motion Estimation Techniques and Their SoC Implementation

Partners: Kocaeli University, Turkey and Seoul National University, Korea

Supported by TUBITAK and Korea Research Foundation (KRF), EEEAG 107E179

Duration: March 2008 - February 2010

Budget for Sabanci University: \$50,000

Contribution: I'm working as a researcher in this project and 1 graduate student in Sabanci University is working under my supervision. Sabanci University is responsible for developing efficient SoC implementations of the low complexity motion estimation techniques developed by our partners.

Completed Projects

Project: Low Power H.264 Video Encoder Design for Portable Applications

Supported by TUBITAK, EEEAG 106E153

Duration: February 2007 - January 2009

Budget: \$120,000

Contribution: I directed this research project and 3 graduate students worked in this project under my supervision. We designed and implemented additional hardware modules, such as mode decision and motion compensation, and built a complete baseline H.264 video encoder system by integrating them to the existing intra frame coder system. We developed low power techniques for reducing the power consumption of this video encoder and assessed their impact on its power consumption.

Project: H.264 Video Encoder Hardware Design

Supported by Sabanci University

Duration: July 2004 - August 2006

Budget: \$70,000

Contribution: I directed this research project and 5 graduate students worked in this project under my supervision. We designed and implemented a baseline H.264 intra frame coder system. The hardware is

implemented in Verilog HDL. The Verilog RTL code works at 71 MHz in a Xilinx Virtex II FPGA and it codes 35 CIF frames per second. The system also includes a software running on an Arm926EJS processor for implementing pre-processing and post-processing functions. The H.264 intra frame coder hardware and software are demonstrated to work together on an Arm Versatile Platform development board. We, in addition, designed and implemented an integer pixel and a sub-pixel accurate motion estimation hardware for H.264 variable block size motion estimation.

5/1997 - 7/1999, Research Assistant

Center for Reliable & High-Performance Computing, University of Illinois at Urbana-Champaign

Project: Test Generation and Test Application Time Reduction Algorithms for VLSI Circuits

Supported by SRC and DARPA

Contribution: New efficient deterministic test pattern generation techniques for combinational and sequential VLSI circuits, new compact test set generation algorithms for combinational circuits under the stuck at, transition delay and CMOS stuck-open fault models, a new design-for-testability technique for reducing the test application time for both standalone and embedded full scan circuits, and a new technique for reducing the test application time for BIST test pattern generators were developed. A state-of-the-art ATPG system incorporating these techniques was designed and implemented in C++. This tool attracted attention from both industry and academia, as it was one of the fastest ATPG tools reported and it generated the most compact test sets reported for combinational circuits.

6/1996 - 9/1996, Staff Research Assistant

Computational Science Methods Group, X Division, Los Alamos National Laboratory, NM, USA

Project: PADMA: PARallel Data Mining Agents For Scalable Text Classification

Supported by Caterpillar and Department of Energy

Contribution: Parallelized the sequential implementation of the hierarchical clustering algorithm, designed and implemented the software architecture of the overall system in C++ on top of the PPFS software, and carried out performance analysis of the system on an IBM SP2.

5/1995 - 5/1996, Research Assistant

Department of Computer Science, University of Illinois at Urbana-Champaign, USA

Project: Portable Parallel File System (PPFS)

Supported by NSF

Contribution: Ported the software to HP-Convex Exemplar and to PVM message passing library, optimized the software written in C++, designed and implemented prefetching infrastructure and sequential prefetching, conducted input/output performance analysis of a chemistry code running on PPFS on an IBM SP2 and an Intel Paragon using the Pablo performance instrumentation and analysis suite to assess the effectiveness of tuning the parallel file system policies to match the application access patterns on the application performance.

7/1992 - 7/1993, Research Assistant

Department of Computer Engineering, Bogazici University, Istanbul, Turkey

Project: A Spelling Checker and Corrector for Turkish to be integrated with ALL-IN-1, Digital Equipment Corporation's Office Automation Package

Supported by Digital Equipment Corporation

Contribution: Participated in the design of the software, and implemented it in Pascal on an IBM PC and later ported it to a VAX 4000-200.

THESES SUPERVISED

PhD Thesis

Low Power H.264 Video Compression Hardware Designs

Mustafa Parlak, Sabanci University, February 2009

Current Position: Postdoctoral Researcher, Georgia Institute of Technology, Atlanta, Georgia, USA

Motion Estimation Based Frame Rate Up-Conversion Hardware Design

Ozgur Tasdizen, Sabanci University, Expected: June 2010

Power Consumption Estimation and Reduction for Video Compression Hardware

Yusuf Adibelli, Sabanci University, Expected: August 2011

Master Thesis

Baseline H.264 Video Encoder Hardware Design

Aydin Aysu, Sabanci University, Expected: August 2010

Low Power Motion Estimation Hardware Designs

Onur Can Ulusel, Sabanci University, Expected: August 2010

One-Bit Transform Based Motion Estimation Hardware Designs

Abdulkadir Akin, Sabanci University, Expected: June 2010

Low Power H.264 Intra Prediction and Mode Decision Hardware Design

Murat Can Kiral, Sabanci University, Expected: June 2010

An Adaptive True Motion Estimation Algorithm for Frame Rate Up-Conversion and Its Hardware Design

Mert Cetin, Sabanci University, August 2009

Dynamic Power Consumption Estimation and Reduction for Full Search Motion Estimation Hardware

Caglar Kalaycioglu, Sabanci University, July 2009

Low Power IEEE 802.11n Low-Density Parity Check (LDPC) Decoder Hardware Design

Merve Peyic, Sabanci University, August 2008

Current Position: ST Ericsson, Istanbul Design Center, Turkey

Sub-pixel Accurate H.264 Motion Estimation Hardware Design

Serkan Oktem, Sabanci University, June 2007

Current Position: CMOSVision, GOSB Technopark, Izmit, Turkey

An Efficient H.264 Intra Frame Coder Hardware Design

Esra Sahin, Sabanci University, August 2006

Current Position: ST Microelectronics, Istanbul Design Center, Turkey

H.264 Intra Frame Coder System Design

Ozgur Tasdizen, Sabanci University, August 2005

Current Position: Vestel Electronic R&D, Istanbul, Turkey

H.264 Motion Estimator Design
Sinan Yalcin, Sabanci University, August 2005
Current Position: Vestel Electronic R&D, Istanbul, Turkey

INDUSTRIAL EXPERIENCE

12/2002 - 8/2003, Principle Staff Engineer (E11)
9/1999 - 11/2002, Senior Staff Engineer (E10)
Multimedia Architecture Lab, Motorola Labs, Schaumburg, IL, USA

Projects:

1/2003 - 8/2003, SoC ASIC for an Image Processing/Vision Application
Contribution: I have participated in the top-level design of this ASIC. I have worked on designing an interface for using a special-purpose coprocessor with an Arm core. I have designed the overall software architecture of a cycle-accurate simulator for a special purpose on-chip memory subsystem, implemented the cycle-accurate simulator for the special purpose cache in this memory subsystem in C++ and integrated the memory subsystem simulator to the system simulation environment. I have worked on designing the memory subsystem using this simulator for performance analysis.

3/2001 - 12/2002, Image Processing Platform SoC ASIC
Contribution: I have involved in every stage of this ASIC design which included an Arm core, various accelerators and peripherals. I was responsible for top-level ASIC development. This involved participating in the top-level design, performance analysis, and determining the pin list, designing and implementing the top-level RTL in Verilog, working with module designers throughout the design process and reviewing their designs, working with DFT team to define the bist and scan insertion strategy and implementing the top-level DFT RTL, synthesizing the top-level design, performing static timing analysis for main modules, writing the top-level testbench and setting up various simulation environments, playing a major role in functional and timing design verification by running simulations and debugging the related problems, interacting with the physical design team to resolve timing problems in the layout, providing support to the emulation team, the evaluation board designer, and the product engineer, generating functional patterns for manufacturing testing, writing test software in C and Arm assembly to verify the basic functionality of the system and Arm core functionality, providing support to the software team and debugging various software problems with hw/sw co-simulation, participating in setting up the chip debugging environment, writing RTL for the FPGA on the evaluation board, and playing a major role in chip testing and debug by testing the top-level asic and various modules and debugging related problems.

9/1999 - 2/2001, MPEG4 Video Codec ASIC
Contribution: I've designed two sub-modules in the encoder, implemented them using Verilog HDL, synthesized and verified them. I've participated in the design of the encoder module and implemented it using Verilog. I've written the control software in a 16-bit Risc Cpu assembly language and integrated this with the rest of the encoder software. I've then verified the encoder module with hardware/software co-simulations.

TEACHING EXPERIENCE

Assistant Professor

Electronics Engineering, Sabanci University, Istanbul, Turkey

EL 310 Hardware Description Languages (Spr 2004, Spr 2005, Spr 2006, Spr 2007, Spr 2008, Spr 2009)

EL 401 VLSI System Design I (Fall 2003, Fall 2004, Fall 2005, Fall 2006, Fall 2007, Fall 2008)

EL 402 VLSI System Design II (Spr 2004, Spr 2005, Spr 2006, Spr 2007, Spr 2008, Spr 2009)

EE 542 Digital Systems Verification and Testing (Spr 2004, Fall 2005, Fall 2007)

EE 634 VLSI Array Processors for Signal Processing (Fall 2004, Fall 2006, Fall 2008)

Visiting Lecturer,

Department of Computer Science, University of Illinois at Urbana-Champaign, USA

CS231 Computer Architecture I (Summer 1998, Summer 1999)

Teaching Assistant

Department of Computer Science, University of Illinois at Urbana-Champaign, USA

CS225 Data Structures and Software Principles (Summer 1997)

CS333 Computer System Organization (Fall 1996, Spring 1997)

CS348 Introduction to Artificial Intelligence (Fall 1994, Spring 1995)

CS257 Introduction to Numerical Analysis (Spring 1994)

Teaching Assistant

Department of Computer Engineering, Bogazici University, Istanbul, Turkey

CMPE450 Software Engineering (Fall 1991)

CMPE223 Data Structures and Algorithms I (Fall 1991)

CMPE224 Data Structures and Algorithms II (Spring 1992)

CMPE100 Computer Programming (Fall 1992, Spring 1993)

PROFESSIONAL ACTIVITIES

Program Committee Member

IEEE Signal Processing and Communication Applications Conference, April 2010, Diyarbakir, Turkey

IEEE Signal Processing and Communication Applications Conference, April 2009, Antalya, Turkey

NASA/ESA Conference on Adaptive Hardware and Systems, June 2008, Noordwijk, Netherlands

NASA/ESA Conference on Adaptive Hardware and Systems, August 2007, Edinburgh, Scotland, UK

NASA/ESA Conference on Adaptive Hardware and Systems, June 2006, Istanbul, Turkey

Reviewer for Conferences

European Conference on Circuit Theory & Design, Design Automation Conference, Int. Conference on Computer-Aided Design, Int. Test Conference, IEEE VLSI Test Symposium

Reviewer for Journals

IEEE Transactions on Circuits and Systems for Video Technology, IEEE Transactions on Circuits and Systems - II, IEEE Transactions on Computer-Aided Design, IEEE Design & Test of Computers, IEEE Signal Processing Letters, ACM Transactions on Design Automation, ACM Transactions on Embedded Computing Systems, Journal of Electronic Testing

Reviewer for Turkish Research Funding Agencies (TUBITAK (The Scientific and Technological Research Council of Turkey), TTGV (Technology Development Foundation of Turkey), TUSIAD (Turkish Industrialists and Businessmen Association))

Reviewer and Project Monitor, TTGV Industry R&D Projects, 2004-present

Reviewer and Project Monitor, TUBITAK Industry R&D Projects, 2005-present

Panelist and Project Monitor, TUBITAK University Research Projects, 2007-present

Reviewer for TUBITAK, TTGV and TUSIAD Technology Awards, 2009

Faculty of Engineering and Natural Sciences, Sabancı University

Microelectronics Program Coordinator, March 2004 – March 2006

Electronics Engineering Program Co-Coordinator, April 2006 – October 2008

PhD Qualification Exam Committee Member, November 2008 -

Proj102 Freshman Project Course Coordinator, Fall2005 - Spr2006

Proj102 Freshman Project Course Committee Member, Fall2006 - Spr2007

Senior Graduation Project Supervisor of 35 Undergraduate Students

Thesis Defense Committee Member of 11 MS students

Qualification Exam Committee Member of 7 PhD students

Reviewer for Istanbul Technical University Scientific Research Projects, 2009

Committee Member for Electrical and Electronics Engineering Department, Bogazici University

Thesis Defense Committee of 1 MS student, 2008

Qualification Exam Committee of 1 PhD student, 2008

Committee Member for Electronics and Telecommunications Engineering Department, Kocaeli University

Thesis Defense Committee of 1 PhD student, 2008

Qualification Exam Committee of 1 PhD student, 2009

Member of Fellowships, Assistantships, and Admissions Committee, Department of Computer Science, University of Illinois at Urbana-Champaign, 1996-1997

AWARDS and HONORS

Listed in Marquis Who's Who in the World, 2010

My publications received more than 600 citations according to Web of Science, September 2009

Bravo Awards for outstanding contributions to MPEG4 Video Codec ASIC and Image Processing Platform SoC ASIC, Motorola Labs, Illinois, USA, 2001 and 2002

W. J. Poppelbaum Memorial Award for Excellent Research in Computer Hardware, Department of Computer Science, University of Illinois at Urbana-Champaign, 1999

TUBITAK NATO Science Fellowship Award for Graduate Studies in USA, 1993

Undergraduate Education Scholarship from Istanbul Chamber of Industry, 1988-1991

Excellence Scholarship from AY-TEST Periodical (because of my score in the University Entrance Exam), 1986

Scored 664.138 in Mathematics and Natural Sciences (which was enough to register to any Department in Engineering and Medicine in all Universities in Turkey) in the University Entrance Exam in Turkey, 1986

GPA: 9.88 (over 10) and Rank: 1st in the School, Affan Kitapcioglu High School, Trabzon, Turkey, 1986

Incitement Award in Mathematics Competition organized by TUBITAK among High School Senior Students in Turkey, 1986

REFEREED PUBLICATIONS

JOURNALS (SCI)

Dynamically Variable Step Search Motion Estimation Algorithm and a Dynamically Reconfigurable Hardware for Its Implementation

Ozgur Tasdizen, Halil Kukner, Abdulkadir Akın, Ilker Hamzaoglu
IEEE Transactions on Consumer Electronics, vol. 55, no. 3, August 2009

Efficient Hardware Implementations of Low Bit Depth Motion Estimation Algorithms

Anıl Celebi, Oguzhan Urhan, Ilker Hamzaoglu, Sarp Erturk
IEEE Signal Processing Letters, vol. 16, no. 6, pp. 513-516, June 2009

High Performance Hardware Architectures for One Bit Transform Based Motion Estimation

Abdulkadir Akın, Yigit Dogan, Ilker Hamzaoglu
IEEE Transactions on Consumer Electronics, vol. 55, no. 2, pp. 941-949, May 2009

An All Binary Sub-Pixel Motion Estimation Approach and its Hardware Architecture

Anıl Celebi, Orhan Akbulut, Oguzhan Urhan, Ilker Hamzaoglu, Sarp Erturk
IEEE Transactions on Consumer Electronics, vol. 54, no. 4, pp. 1928-1937, November 2008

A Novel Computational Complexity and Power Reduction Technique for H.264 Intra Prediction

Mustafa Parlak, Yusuf Adıbelli, Ilker Hamzaoglu
IEEE Transactions on Consumer Electronics, vol. 54, no. 4, pp. 2006-2014, November 2008

An Efficient H.264 Intra Frame Coder System

Ilker Hamzaoglu, Ozgur Tasdizen, Esra Sahin
IEEE Transactions on Consumer Electronics, vol. 54, no. 4, pp. 1903-1911, November 2008

Low Power H.264 Deblocking Filter Hardware Implementations

Mustafa Parlak, Ilker Hamzaoglu
IEEE Transactions on Consumer Electronics, vol. 54, no. 2, pp. 808-816, May 2008

Test Set Compaction Algorithms for Combinational Circuits

Ilker Hamzaoglu and Janak H. Patel
IEEE Transactions on Computer-Aided Design, vol. 19, no. 8, pp. 957-963, August 2000

New Techniques for Deterministic Test Pattern Generation

Ilker Hamzaoglu and Janak H. Patel
Journal of Electronic Testing, vol. 15, no. 1/2, pp. 63-73, October 1999

BOOK CHAPTERS

Ilker Hamzaoglu and Huseyin Simitci
Performance Analysis of Tape Libraries for Supercomputing Environments
High Performance Computing Systems and Applications
Chapter 54, Pages 559-574, ISBN 978-0-7923-7774-0, Springer, 2002

INTERNATIONAL CONFERENCES

Low Power Digital Hardware Design

Caglar Kalaycioglu, Onur Ulusel, and Ilker Hamzaoglu
Low Power Techniques for Motion Estimation Hardware
19th International Conference on Field Programmable Logic and Applications, September 2009, Prague, Czech Republic

Merve Peyic, Hakan Baba, Ilker Hamzaoglu and Mehmet Keskinöz
Low Power IEEE 802.11n LDPC Decoder Hardware
16th IFIP/IEEE International Conference on VLSI-SoC, October 2008, Rhodes Island, Greece

Mustafa Parlak and Ilker Hamzaoglu
A Low Power Implementation of H.264 Adaptive Deblocking Filter Algorithm
NASA/ESA Conference on Adaptive Hardware and Systems, August 2007, Edinburgh, Scotland, UK
(This paper received Best Paper Prize in Adaptive and Reconfigurable Circuits for Multimedia Category)

Digital Hardware Design for Video Processing and Compression

Abdulkadir Akin, Yigit Dogan, and Ilker Hamzaoglu
A High Performance Hardware Architecture for One Bit Transform Based Motion Estimation
12th Euromicro Conference on Digital System Design, August 2009, Patras, Greece

Ozgur Tasdizen and Ilker Hamzaoglu
A Reconfigurable Frame Interpolation Hardware Architecture for High Definition Video
12th Euromicro Conference on Digital System Design, August 2009, Patras, Greece

Ozgur Tasdizen, Halil Kukner, Abdulkadir Akin and Ilker Hamzaoglu
A High Performance Reconfigurable Motion Estimation Hardware Architecture
Design, Automation and Test in Europe (DATE) Conference, April 2009, Nice, France

Ozgur Tasdizen, Abdulkadir Akin, Halil Kukner, Ilker Hamzaoglu and Fatih Ugurdag
High Performance Hardware Architectures for a Hexagon-Based Motion Estimation Algorithm
16th IFIP/IEEE International Conference on VLSI-SoC, October 2008, Rhodes Island, Greece

Ilker Hamzaoglu, Ozgur Tasdizen and Esra Sahin
An Efficient H.264 Intra Frame Coder System Design
15th IFIP International Conference on VLSI-SoC, October 2007, Atlanta, Georgia, USA

Serkan Oktem and Ilker Hamzaoglu
An Efficient Hardware Architecture for Quarter-Pixel Accurate H.264 Motion Estimation
10th Euromicro Conference on Digital System Design, August 2007, Lübeck, Germany

Esra Sahin and Ilker Hamzaoglu
An Efficient Intra Prediction Hardware for H.264 Video Decoding
10th Euromicro Conference on Digital System Design, August 2007, Lübeck, Germany

Esra Sahin and Ilker Hamzaoglu
An Efficient Hardware Architecture for H.264 Intra Prediction Algorithm
Design, Automation and Test in Europe (DATE) Conference, April 2007, Nice, France

Sinan Yalcin and Ilker Hamzaoglu
A High Performance Hardware Architecture for Half-Pixel Accurate H.264 Motion Estimation
14th IFIP International Conference on VLSI-SoC, October 2006, Nice, France

Mustafa Parlak and Ilker Hamzaoglu
An Efficient Hardware Architecture for H.264 Adaptive Deblocking Filter Algorithm
NASA/ESA Conference on Adaptive Hardware and Systems, June 2006, Istanbul, Turkey

Ozgur Tasdizen and Ilker Hamzaoglu
A High Performance and Low Cost Hardware Architecture for H.264 Transform and Quantization Algorithms
13th European Signal Processing Conference, September 2005, Antalya, Turkey

Esra Sahin and Ilker Hamzaoglu
A High Performance and Low Power Hardware Architecture for H.264 CAVLC Algorithm
13th European Signal Processing Conference, September 2005, Antalya, Turkey

Sinan Yalcin, Hasan F. Ates, and Ilker Hamzaoglu
A High Performance Hardware Architecture for an SAD Reuse based Hierarchical Motion Estimation Algorithm for H.264 Video Coding
15th Int. Conference on Field Programmable Logic and Applications, August 2005, Tampere, Finland

Computer-Aided Testing of Digital Systems

(The following 6 papers and their two journal paper versions received more than 500 citations according to Web of Science, September 2009)

I. Hamzaoglu and J. H. Patel
Deterministic Test Pattern Generation Techniques for Sequential Circuits
International Conference on Computer-Aided Design, November 2000, San Jose, California, USA

I. Hamzaoglu and J. H. Patel
Reducing Test Application Time for Built-in-Self-Test Test Pattern Generators
IEEE VLSI Test Symposium, April 2000, Montreal, Canada

I. Hamzaoglu and J. H. Patel
Reducing Test Application Time for Full Scan Embedded Cores
Int. Symposium on Fault-Tolerant Computing, pp. 260-267, June 1999, Madison, Wisconsin, USA

I. Hamzaoglu and J. H. Patel
Test Set Compaction Algorithms for Combinational Circuits
Int. Conference on Computer Aided Design, pp. 283-289, November 1998, San Jose, California, USA

I. Hamzaoglu and J. H. Patel
Compact Two-Pattern Test Set Generation for Combinational and Full Scan Circuits
Int Test Conference, pp. 944-953, October 1998, Washington, D.C., USA

I. Hamzaoglu and J. H. Patel
New Techniques for Deterministic Test Pattern Generation
IEEE VLSI Test Symposium, pp. 446-452, April 1998, Monterey, California, USA

Parallel Processing

I. Hamzaoglu and H. Simitci
Performance Analysis of Tape Libraries for Supercomputing Environments
Int. Symposium on High Performance Computing Systems and Applications, pp. 447-462, June 1999,
Kingston, Ontario, Canada

(The following 3 papers received more than 50 citations according to Web of Science, September 2009)

H. Kargupta, B. Stafford, and I. Hamzaoglu
Web Based Parallel/Distributed Medical Data Mining Using Software Agents
American Medical Informatics Association Fall Symposium, October 1997, Nashville, Tennessee, USA

H. Kargupta, I. Hamzaoglu, and B. Stafford
Scalable, Distributed Data Mining Using an Agent Based Architecture
Int. Conference on Knowledge Discovery and Data Mining, pp. 211-214, August 1997, Newport Beach,
California, USA

H. Kargupta, I. Hamzaoglu, B. Stafford, V. Hanagandi, and K. Buescher
PADMA: PARallel Data Mining Agents for Scalable Text Classification
High Performance Computing Conference, pp. 290-295, April 1997, Atlanta, Georgia, USA

NATIONAL CONFERENCES

Anil Celebi, Oguzhan Urhan, Sarp Erturk, Ilker Hamzaoglu, Gunhan Dunder
MVBLA Based Design of Constrained 1-Bit Transform Based Motion Estimation Algorithm
16th IEEE Signal Processing and Communication Applications Conference, April 2008, Aydin, Turkey

Ilker Hamzaoglu and Selahattin Kuru
Machine Translation from Turkish to Other Turkic Languages
Artificial Intelligence and Neural Networks Symposium, pp. 135-145, July 1993, Istanbul, Turkey

H. L. Akin, S. Kuru, T. Gungor, I. Hamzaoglu, and D. Arbatli
A Spelling Checker and Corrector for Turkish
Artificial Intelligence and Neural Networks Symposium, pp. 113-120, July 1993, Istanbul, Turkey

TECHNICAL REPORTS

J. V. Huber, C. L. Elford, D. A. Reed, A. A. Chien, D. Blumenthal, I. Hamzaoglu, A. J. Lavery, M. P.
Mesnier, and J. P. Oly
Users' Guide for PPFS: A High-Performance Portable Parallel File System
Department of Computer Science, University of Illinois at Urbana-Champaign, USA, 1996