Domain control of carrier density at a semiconductor-ferroelectric interface

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Abstract

Control of charge carrier distribution in a gated channel via a dielectric layer is currently the state of the art in the design of integrated circuits such as field effect transistors. Replacing linear dielectrics with ferroelectrics would ultimately lead to more energy efficient devices as well as the added advantage of the memory function of the gate. Here, we report that the channel-off/channel-on states in a metal/ferroelectric/semiconductor stack are actually transitions from a multi domain state to a single domain state of the ferroelectric under bias. In our approach, there is no apriori assumption on the single or multi-domain nature of the ferroelectric layer that is often neglected in works discussing the ferroelectric-gate effect on channel conductivity interfacing a ferroelectric. We also predict that semiconductor/ferroelectric/semiconductor stacks can function at even lower gate voltages than metal/ferroelectric/semiconductor stacks when an n-type semiconductor is placed between the ferroelectric and the gate metal. Our results suggest the ultimate stability of the multidomain state whenever it interfaces a semiconductor electrode and that a switchable single domain state may not be necessary to achieve effective control of conductivity in a p-type channel. Finally, we discuss some experimental results in the literature in light of our findings.

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