Lab Assignment 1

This laboratory assignment introduces the construction and simulation of simple VHDL models. Follow the steps:

1. Create VHDL models for different types of full adders. Recall that a regular full adder realizes the following function:

   2c + s = x + y + z

   where x, y, and z are input signals and s and c are output signals. There are three other types of full adders. They realize the following functions, respectively:

   FA1: 2c - s = -x + y + z
   FA2: -2c + s = -x - y + z
   FA3: -2c - s = -x - y – z

   a. Set the gate delays 3 ns for the XOR gates and to 2ns for other gates. Include IEEE library and use std_logic_1164 package.
   b. Write the entity description. Use std_logic and std_logic_vector for the input and output signals
   c. Write the architecture description for each of three full adders.

   For three types of full adders (i.e. FA1, FA2, FA3) repeat the following steps.

2. Compile and load the model for simulation using your VHDL simulator toolset.
3. Generate a waveform on each of the input signals.
4. Run the simulation for 40 ns and trace (i) the input signals (ii) internal signals (iii) outputs
5. Pick an event on one of the input signals. Record the propagation of the effect of this event through the signal trace. Study the trace and make sure that the model is operating correctly.
6. Repeat this example, only this time do not initialize one of the input signals. What does the resulting trace look?

You are required to demonstrate Steps 4, 5 and 6 of the assignment to the TA.