VHDL Introduction

EL 310
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What is VHDL ?

- VHDL stands for ***VHSIC Hardware Description Language***
- VHSIC = ***Very High-Speed Integrated Circuit***
- Initialized by US DoD as a sponsored program
- Standardized as IEEE 1076-1987 in 1987
- Revised in 1993 (used in this course)
- Other HDLs: Verilog and ABEL
- DoD requires that VHDL descriptions be delivered for all ASICs.
- every major CAD vendors supports VHDL

VHDL Provides

- Portability
- Interoperability across vendors
- Code reuse
- Distributed design
- Reliable design process
- Minimized design time and cost

Programming Languages vs. HDLs

- Procedural programming languages (C or Pascal) typically provide procedures for
  - Performing a computation (e.g. matrix multiplication)
  - Manipulating data (e.g. sorting)
- Hardware description language is used to describe a digital system
  - Simulate the behavior of the system without actually constructing the system
  - Synthesis compilers can use the description to actually build a digital system implementing this behavior
  - VHDL is primarily used for digital system design

Why Describing Systems ?

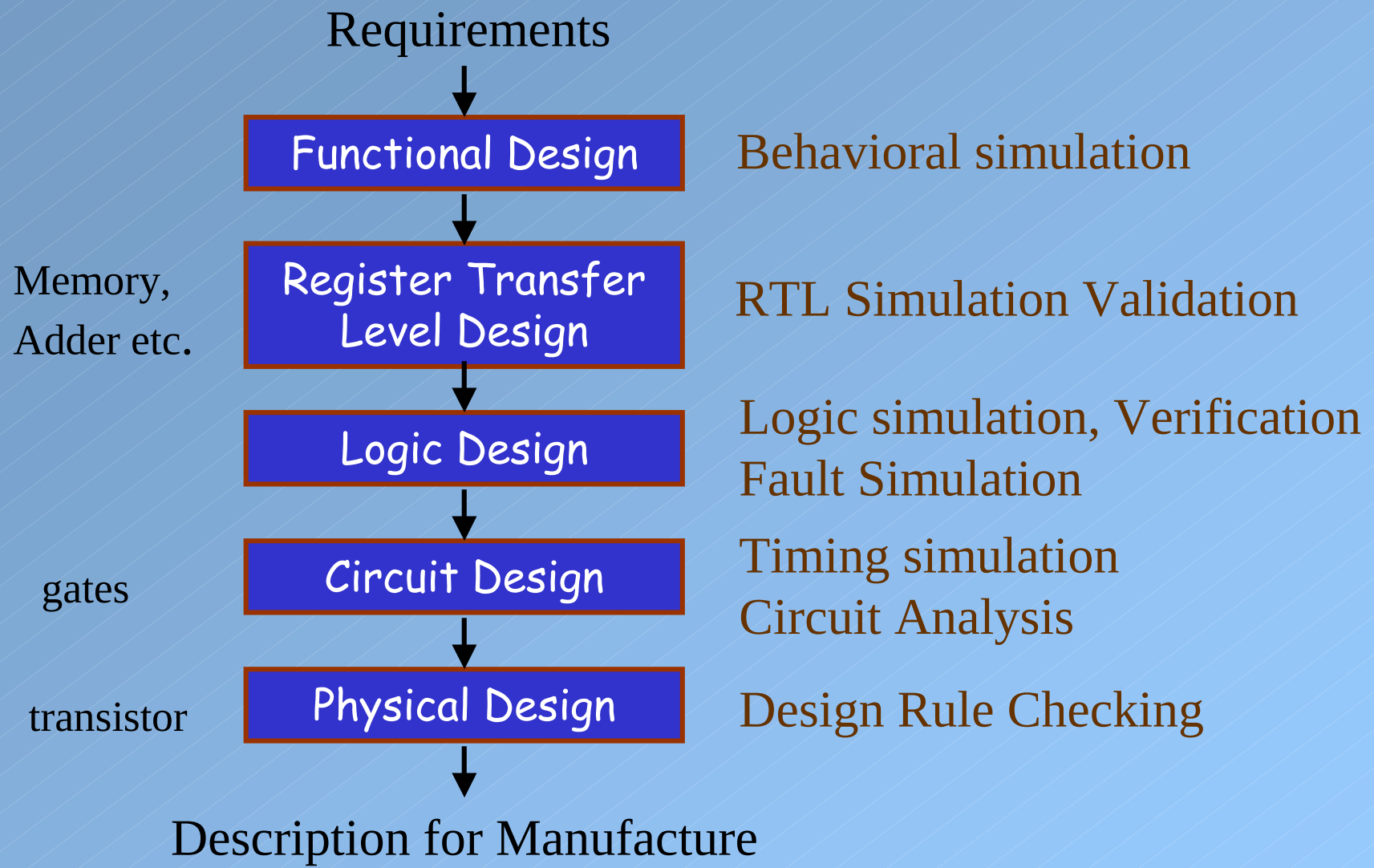
- Design specification
  - Unambiguous definition of components and interfaces in a large design.
- Design Simulation
  - Verify system/subsystem/chip performance prior to implementation
- Design Synthesis
  - Automated generation of hardware implementing the digital system

Describing Digital System

Different levels of abstractions

- Application Level
- System Level
- Architecture Level
- Device or Circuit Level

Design Flow:Top-down approach

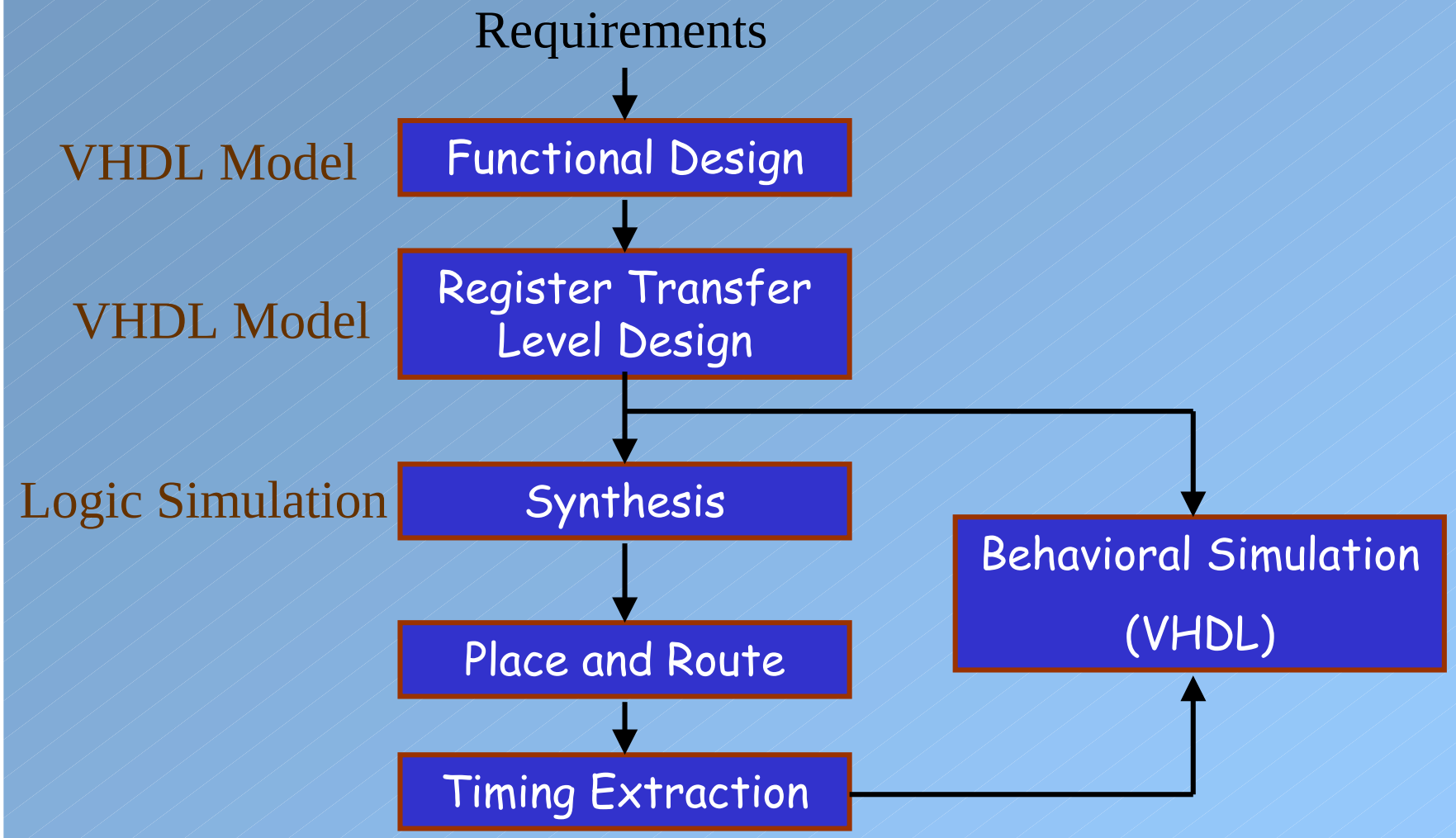


ASIC Design Process

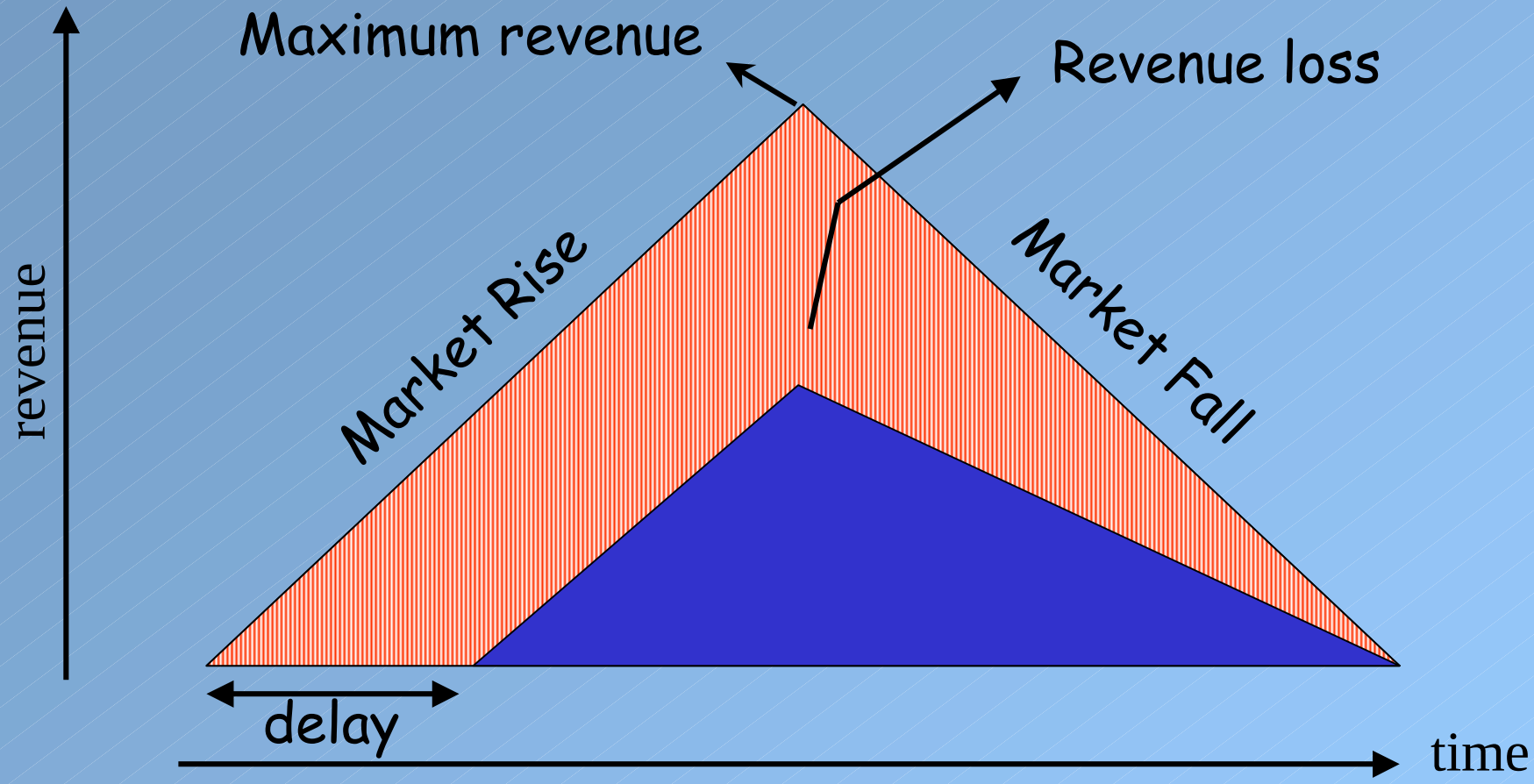
Levels of Abstraction

- Design tools support to perform simulation at each level
  - These simulations are for anticipating behavior, physical properties, and performance of the circuit
  - Simulation at lower levels offers more accurate predictions, but takes longer.
  - If design errors are discovered at lower levels, changes in the design to correct faults may be expensive ➔longer development times
  - Having simulation capability at different level helps detect and correct the design errors at earlier stages

Synthesis Design Flow for FPGA

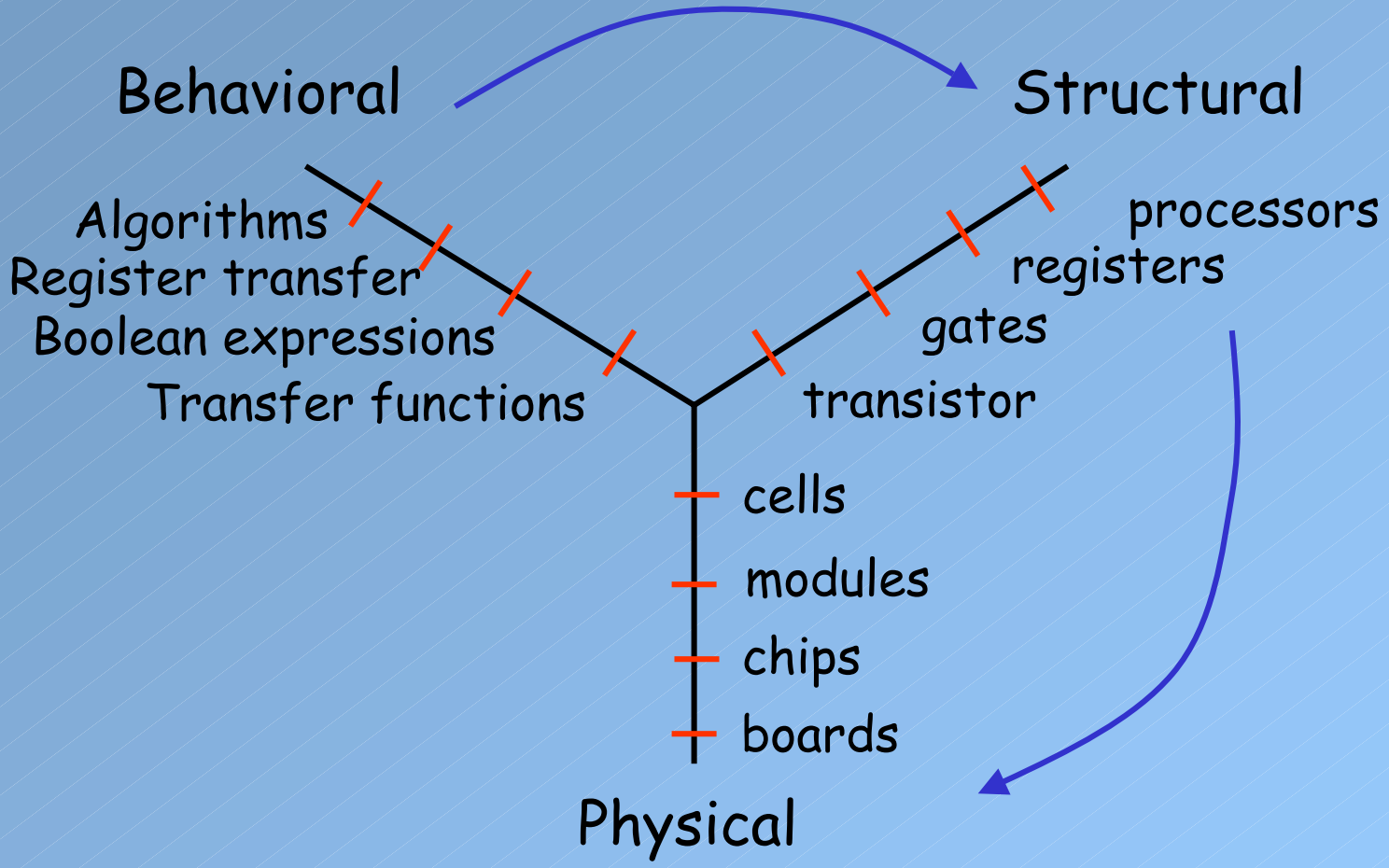


Need of Shorter Design Cycle?



- The first 10%-20% of the design cycle can determine 70%-80% of final system cost.
- 5%-10% of design cycle is spent on studying and formulating requirements, whereas 70% of manufacturing costs are affected by customer requirements.

The Role of HDL -1: Y-Chart



- Point tools are good for a single aspect of design
- Transfer information btw these tools is hard

The Role of HDL - 2

- Digital design is structured around a hierarchy of representations
- HDLs can describe distinct aspects of a design at multiple levels of abstraction
- Interoperability : tools that are designed for different aspects of design can transfer information to each other
- Technology independence: a design environment that is independent of a particular target technology
  - We do not have to describe a system at gate level

The Role of HDL - 3

- Timing analysis
  - Prior to physical design, a detailed timing information can be extracted via simulation to ensure that performance requirements can be met.
- Hardware/software co-design (or prototyping)
  - simulate a processor architecture for functional accuracy so that application software developers can start coding before the actual chip is produced.
- Design re-use
  - Libraries of VHDL models of components
  - They can be shared exactly as software libraries
  - You can include a highly optimized component in your project

Summary

- HDL for describing digital systems
  - specification
  - simulation
  - synthesis
- Description at various levels of abstraction
  - system, architectural, RTL, logic, gate, etc.
  - VHDL integrates point tools into a cohesive design process
- VHDL is independent of technology
- faster time-to-market