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EDUCATION

Ph.D. in Computer Science and Engineering, May 2007
The Pennsylvania State University, University Park, PA.

Master of Science in Computer and Information Science and Engineering, August 2002
University of Florida, Gainesville, FL.

Bachelor of Science in Computer Engineering, June 2000
Bogazici University, Istanbul, Turkey

INDUSTRIAL AND ACADEMIC EXPERIENCE

- **Professor**, **Sabanci University,** Computer Science and Engineering and Electronics Engineering Programs, Faculty of Engineering and Natural Sciences, Istanbul, Turkey, February 2024 – Present.
- **Professor**, **Bilkent University,** Computer Engineering Department, Ankara, Turkey, November 2018 – January 2024.
- **Adjunct Professor, North Carolina State University,** Department of Computer Science (CSC), School of Engineering, Raleigh, North Carolina, July 2018 – Present.
- **Visiting Associate Professor, North Carolina State University,** Department of Computer Science (CSC), School of Engineering, Raleigh, North Carolina, January 2018 – August 2018.
- **Associate Professor**, **Bilkent University,** Computer Engineering Department, Ankara, Turkey, June 2013 – October 2018.
- **Visiting Associate Professor, Arizona State University,** Department of Computer Science and Engineering, School of Computing, Informatics and Decision Systems Engineering, Tempe, Arizona, July 2014 – January 2015.
- **Assistant Professor**, **Bilkent University,** Computer Engineering Department, Ankara, Turkey, January 2008 – May 2013.
- **Senior Researcher**, **NEC Labs America**, Princeton, New Jersey, January 2011 – September 2011.
- **Visiting Researcher**, **INRIA**, Paris, France, June 2009 – August 2009, ALCHEMY group (Architectures, Languages and Compilers to Harness the End of Moore Years): Optimization using Polyhedral Model.
- **Senior Software Optimization Engineer**, **Intel Corporation**, Cellular and Handheld Group **-** Marvell, April 2006 – January 2008, Chandler, Arizona: Senior Software Optimization Engineer.
- **Research Associate**, Processor Architecture Laboratory (LAP), **Swiss Federal Institute of Technology of Lausanne (EPFL)**, July 2003 – August 2003, Lausanne, Switzerland: Optimization of a MachSUIF compiler backend for the ARM architecture.
- **Research Assistant/Teaching Assistant**, CSE Department, August 2002 – August 2006, Pennsylvania State University, State College, Pennsylvania.
- **Teaching Assistant**, Computer and Information Science and Engineering Department, August 2000 – May 2002, University of Florida, Gainesville, Florida.

HONORS/AWARDS

- Best Paper Award, Design and Test Symposium (DTS'20), 2020.
- Bilkent University Distinguished Teaching Award, 2019.
- Science Academy's Young Scientist Award (BAGEP), 2018
- Parlar Foundation Young Investigator Award, 2018
- European Network of Excellence on High Performance and Embedded Architecture and Compilation (HiPEAC) Paper Award, 2016.
- Best Paper Award from The 18th Euromicro Conference on Digital Systems Design, Funchal, Madeira, Portugal in August 26-28, 2015.

- Turkish Academy of Sciences (TÜBA) Associate Member, 2015.
- Fulbright Senior Researcher Award, 2014.
- Intel Research Award, 2013.
- Turk Telekom Research Collaboration Award, 2012.
- Associate Professor (Doçent) title from Inter-University Council (UAK) of Turkey, June 2011.
- IBM Faculty Award, 2009.
- European Network of Excellence on High Performance and Embedded Architecture and Compilation (HiPEAC) Paper Award, 2009.
- EC FP7 Marie Curie Fellowship, 2009.
- Tubitak (Turkish NSF) Incentive Award for European Union FP7 Marie Curie IRG project, 2009.
- The most popular paper from ACM's refereed journals and conference proceedings downloaded, October 2006 (Communications of the ACM, January 2007/Vol. 50, No. 1).
- Best Paper Award from the Twelfth International Conference on Parallel and Distributed Systems (ICPADS'06), Minneapolis, Minnesota, June 2006.
- Nominated for Best Paper Award in DAC-2006 and DAC-2004.

TEACHING EXPERIENCE

- Courses at Sabanci:
    - EE48008/EE58008 – Special Topics in EE: Heterogeneous Computing and System-on-Chip Design (Spring 24)
- Courses at Bilkent:
    - CS 101 – Algorithms and Programming I (Spring 10, Fall 21, 22, 23)
    - CS 102 – Algorithms and Programming II (Fall 20, Summer 08, 10, 13, 15, 16, 17, 21, Spring 12, 13, 14, 15, 16)
    - CS 223 – Digital Design (Fall 08, 10, 16, 19, Spring 11)
    - CS 224 – Computer Organization (Spring 08, 09, 10, 11, 15, 16, 17, 20, 21, 22, 23 Fall 17, 18, 19)
    - CS 342 – Operating Systems (Spring 17, 19, 21, 22, Fall 15, 17, 18)
    - CS 423 – Computer Architecture (Fall 09, Spring 12)
    - CS 426 – Parallel Computing (Spring 12, 13, 14, 19, 20, Fall 15, 16, 17, 20, 21, 22, 23, Summer 21)
    - CS 432 – Machine to Machine Systems (Spring 14, 15, 19, 20, 21)
    - CS 541 – Chip Multiprocessors (Spring 08, 09, Fall 11, 12, 13)
    - CS 590/690 – Research Topics (Fall 08, Spring 10, Fall 10, 23)
    - GE 401-2 Innovative Product Design and Development I-II (Fall 09,11,12, Spring 10,12)
- Past Courses:
    - CSE 203 - Business Programming (Pennsylvania State University, Fall 02)
    - CSE 201C - C++ Programming for Eng. (Pennsylvania State University, Spring 03)
    - COP 3100 - Applications of Discrete Structures (U. Of Florida, Fall 00, Spring 01)
    - COP5725 - Graduate- Database Management Systems (U. Of Florida, Fall 01, Spring 02)
    - COP4720 - Database Management Systems (U. Of Florida, Fall 01, Spring 02)

RESEARCH INTERESTS

- **Accelerators:** Accelerator Technologies, Heterogeneous Systems, Manycore Accelerators
- **Parallel Systems / High Performance Computing:** Heterogeneous Clusters, GPU-based Systems, Efficient Parallelization, Resource Management, Cloud Computing, Parallel Programming
- **Processor Architecture:** Multicore Processors, Computer Organization, Reliability-Aware 3D Chip Multiprocessor Design, Heterogeneous Chip Multiprocessors, Network On Chip Architectures
- **Compilers:** Automatic Parallelization, Dataflow Analysis, Programming Languages, Optimizing Compilers, Memory Optimization

RESEARCH PROJECTS

- Using Machine Learning Methods to Select GCC Compiler Flags To Optimize Runtime, 2022-2024, Funded by **Huawei - TUBITAK** – Teydeb 1505 - 5210111.
- Selecting Optimal Compiler Flags Through Machine Learning Techniques, 2021-2024, Funded by **Huawei.**
- Processor Design for Graph Applications, 2020-2023, Funded by **TUBITAK** 1001 - 119E559.
- Deep Neural Network Accelerator Design, 2019-2021, Funded by **ASELSAN-SAYP.**
- Processor Emulator for Safety Critical Applications, 2017-2019, Funded by **Turkish Aviation Industries (TAI)**.
- A High Level Design Methodology for Developing Graph Algorithms on Xeon + FPGA Platforms, 2017-2020, Funded by **Intel Corporation**, (with Assist. Prof. Mustafa Ozdal, Bilkent University).
- Safe Computer Design, 2015-101, 2015-2017, Funded by **ASELSAN.**
- Software and Hardware Solutions for Safety Critical Applications, 2016-18, Funded by **TUBITAK.**
- Using Accelerator Technologies in Graph Parallel Applications, 2013-2015, Funded by **Intel Corp**.
- CUDA Research Center (CRC), 2013 - 2017, Funded by **NVIDIA**.
- Hardware/Software Mechanisms to Enhance the Effectiveness of Directory Based Cache Coherence in Tiled Chip Multiprocessors (**TUBITAK** - 113E258), 2013-2015, (with Assoc. Prof. Ismail Kadayif, Canakkale Onsekiz Mart University).
- Reliability-Aware Network on Chip (NoC) Architecture Design (**TUBITAK** - 112E360), 2013-2015, (with Assoc. Prof. Suleyman Tosun, Ankara University).
- Utilizing Accelerator Technologies in the Cloud, Funded by **TÜRK TELEKOM**, 2012-2013.
- Developing Techniques for Automatic Parallelization, Funded by European Network of Excellence on High Performance and Embedded Architecture and Compilation (**HiPEAC**), 2010-2011, (with Prof. Michael O'Boyle, University of Edinburgh)
- Heterogeneous Chip Multiprocessor Design (HTCMP), Funded by European Commission (EC) **FP7**-PEOPLE MARIE CURIE ACTIONS, 2009 – 2013.
- Energy Efficient Application Mapping onto Network-on-Chips with Different Topologies, Funded by The Scientific & Technological Council of Turkey (**TUBITAK** – 108E233), 2009 – 2012, (with Asst. Prof. Suleyman Tosun, Ankara University).
- Utilizing Heterogeneous CMPs through Efficient Parallelization, Funded by **IBM**, 2009-2010.
- Parallelizing for IBM Cell, Funded by EC **FP7** HPC-Europa2, 2009-2010.

PROFESSIONAL ACTIVITIES

- Turkish Academy of Sciences Associate member.
- IEEE Senior member.
- ACM member.
- HiPEAC (European Network of Excellence on High Performance and Embedded Architecture and Compilation) member.
- GSRC (Gigascale Systems Research Center) member.
- Steering Committee Member
    - International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), 2015-Present.
    - International Conference on Supercomputing (ICS), 2016-Present.
- Program/General Chair
    - DSD 2023 – Special Sessions Chair, Digital System Design, Durres, Albania, Sep 2023.
    - MSE 2017 – General Chair, Microsystems Education, Banff, Canada, May 2017.
    - ICS 2016 – General Chair, 30th International Conference on Supercomputing, Istanbul, Turkey, June 2016.
    - ASPLOS 2015 – General Chair, 20th International Conference on Architectural Support for Programming Languages and Operating Systems, Istanbul, Turkey, March 2015.
    - MSE 2015 – Program Chair, Microsystems Education, Pittsburgh, Pennsylvania, May 2015.
    - MEDIAN 2014 – Program Co-Chair, Manufacturable and Dependable Multicore Architectures at Nanoscale, Dresden, Germany, March, 2014.
    - MSE 2013 - Registration Chair, Microsystems Education, Austin, Texas
- Program Committee Member
    - ICCD 2020, DSD 2020, DTS 2020, ICS 2020, WAICA 2020, IPDPS 2020
    - ITC 2019, DSD 2019, GLSVLSI 2019, IPDPS 2019, ISCA 2019, HPCA 2019
    - ICCD 2018, DSD 2018, ASAP 2018, HPCA 2018,
    - ICCD 2017, DSD 2017
    - DSD 2016, ASAP 2016
    - MICRO 2015, IPDPS 2015, HiPC 2015, DSD 2015, PPAM 2015, ASAP 2015, APPT 2015
    - MICRO 2014, IDT 2014, COSMIC 2014, DSD 2014, VLSI Design 2014
    - IDT 2013, DSD 2013, RAPIDO 2013, DFR 2013, PPAM 2013
    - IPDPS 2012, DSD 2012, RAPIDO 2012, DFR 2012
    - MSE 2011, IPDPS 2011
    - ICC 2010, Cost HPCCE 2010, YKGS'2010, UYMK'2010, DSD 2010, NSS 2010
    - DSD 2009, NSS 2009, ISCIS 2009
- Refereeing for Scholarly and Professional Journals
    - IEEE Transactions on Computers
    - IEEE Transactions on Parallel and Distributed Systems
    - IEEE Transactions on Computer Aided Design
    - IEEE Signal Processing Magazine
    - IEEE Transactions on Very Large Scale Integration (VLSI) Systems
    - IEEE Transactions on Education
    - ACM Transactions on Design Automation of Electronic Systems
    - ACM Transactions on Embedded Computing Systems
    - ACM Transactions on Architecture and Code Optimization
    - Elsevier Computer Communications
    - Wiley Concurrency and Computation: Practice and Experience
- Reviewer for several conferences: PACT, EMSOFT, ICCD, CASES, DATE, ISLPED, ISPASS, ISCAS, TVLSI, TODAES, TCAD, Computer Architecture Letters, HiPC, etc.

GRADUATE STUDENT SUPERVISION

- Current
  - Yunus Esergün, MS
  - Alperen Kalay, MS
  - Muhammed Yıldırım, MS
  - İlayda Sarıçam, MS
- Completed
  - Hamzeh Ahangari, PhD (2020)
  - Naveed Ul Mustafa, PhD (2018)
  - Utku Gulgec, MS (2023)
  - Melih Peker, MS (2023)
  - Pouria Hasani, MS (2022)
  - Mehmet Ali Semi Yenimol, MS (2022)
  - Nihat Mert Cicek, MS (2021)
  - Kenan Cagri Hirlak, MS (2021)
  - Gulce Pulat, MS (2020)
  - Zulal Bingol, MS (co-advised with C. Alkan, 2020)
  - Kaan Akyol, MS (2019)
  - Funda Atik, MS (2018)
  - Erdem Derebasoglu, MS (2017)
  - Serif Yesil, MS (2016)
  - Azita Nouri, MS (co-advised with C. Alkan) (2016)
  - Mohammad Reza Soltaniyeh, MS (2015)
  - Tuncer Turhan, MS (2014)
  - Habibe Guldamla Ozsema, MS (co-advised with B. Gedik) (2014)
  - Ismail Akturk, MS (2013)
  - Omer Erdil Albayrak, MS (2013)
  - Dilek Demirbas, MS (2011)

UNDERGRADUATE STUDENT SUPERVISION

- Burak Ocalan, 2022
- Serif Yesil, 2012
- Engin Kayraklioglu, 2012
- Mustafa Zengin, 2011
- Kamil Akhuseyinoglu, 2010

PUBLICATIONS

Books:

Memory Hierarchy Design For Chip Multiprocessors: A Compiler Directed Approach (Paperback) by Ozcan Ozturk, VDM Verlag Dr. Müller, December, 2008.

Book Chapters:

1. Workload Clustering for Increasing Energy Savings in MPSoCs, by O. Ozturk, M. Kandemir, and S. H. K. Narayanan,Energy Efficient Distributed Computing Systems, John Wiley & Sons Inc., Editor: Albert Zomaya, ISBN: 978-0-470-90875-4, pages 549--565.
2. Improving Multicore System Performance Through Data Compression, by O. Ozturk and M. Kandemir, Programming Multi-core and Many-core Computing Systems, Book Editors Sabri Pllana and Fatos Xhafa, John Wiley & Sons Inc., In Press.
3. Enabling Network Security in HPC Systems Using Heterogeneous CMPs, by O. Ozturk and S. Tosun, High-Performance Computing on Complex Environments, John Wiley & Sons Inc., Editor: Emmanuel Jeannot and Julius Zilinskas, ISBN: 978-1-118-71205-4, pages 383--401.

Patents:

1. Nishkam Ravi, Tao Bao, Ozcan Ozturk, and Srimat Chakradhar. "A COMPILER FOR X86-BASED MANY-CORE COPROCESSORS", Disclosure 11032a (449-241).

2. Nishkam Ravi, Tao Bao, Ozcan Ozturk, and Srimat Chakradhar. "AN OPTIMIZING COMPILER FOR IMPROVING APPLICATION PERFORMANCE ON MANY-CORE COPROCESSORS", Disclosure 11032b (449-242).

Journals:

1. GateKeeper-GPU: Fast and Accurate Pre-Alignment Filtering in Short Read Mapping, by Zülal Bingöl, Mohammed Alser, Onur Mutlu, Ozcan Ozturk, and Can Alkan. . IEEE Transactions on Computers, Accepted. **[SCI]**

2. HLS-based High-Throughput and Work-Efficient Synthesizable Graph Processing Template Pipeline, by Hamzeh Ahangari, Muhammet Mustafa Ozdal, and Ozcan Ozturk. ACM Transactions on Embedded Systems (TECS) Volume 22, Issue 2, Article No. 34. https://doi.acm.org?doi=3529256. **[SCI]**

3. Architecture for safety–critical transportation systems, by Hamzeh Ahangari, Yusuf İbrahim Özkök, Asil Yıldırım, Fatih Say, Funda Atik, Ozcan Ozturk. Microprocessors and Microsystems, Volume 98, 2023, 104818, ISSN 0141-9331, https://doi.org/10.1016/j.micpro.2023.104818. **[SCI-E]**

4. Energy Efficient Boosting of GEMM Accelerators for DNN via Reuse, by Nihat Mert Cicek, Xipeng Shen, Ozcan Ozturk. ACM Transactions on Design Automation of Electronic Systems (TODAES), Volume 27, Issue 5, Article 43 (September 2022), https://doi.org/10.1145/3503469 **[SCI]**

5. General Reuse-Centric CNN Accelerator, by Nihat Cicek, Lin Ning, Ozcan Ozturk, Xipeng Shen. IEEE Transactions on Computers, vol. 71, no. 4, pp. 880-891, 1 April 2022, doi: 10.1109/TC.2021.3064608. **[SCI]**

6. Scheduling for Heterogeneous Systems in Accelerator-Rich Environments, by Serif Yesil and Ozcan Ozturk, The Journal of Supercomputing, 78, 200–221 (2022). https://doi.org/10.1007/s11227-021-03883-5. **[SCI-E]**

7. Recent Advances in Autonomous Vehicle Solutions in the Digital Continuum, by Ozcan Ozturk, Sabri Pllana, Smaïl Niar, and Kaoutar El Maghraoui. Computing, 104, 459-460, 2022, DOI: 10.1007/s00607-021-01024-7. **[SCI-E]**

8. ILP Formulation and Heuristic Method for Energy-aware Application Mapping on 3D-NoCs, by Yigitcan Nalci, Pinar Kullu, Suleyman Tosun, and Ozcan Ozturk.The Journal of Supercomputing. DOI: 10.1007/s11227-020-03365-0, July 2020. **[SCI-E]**

9. Power-efficient reliable register file for aggressive-environment applications, by Ihsen Alouani, Hamzeh Ahangari, Ozcan Ozturk, and Smail Niar. IET Computers & Digital Techniques, Volume 14, Issue 1, January 2020, p. 1–8. DOI: 10.1049/iet-cdt.2018.5047. **[SCI-E]**

10. Exploiting Architectural Features of a Computer Vision Platform Towards Reducing Memory Stalls, Naveed Ul Mustafa, Martin J.O'Riordan, Stephen Rogers, Ozcan Ozturk, Journal of Real-Time Image Processing, Volume 17, 2020. DOI: 10.1007/s11554-018-0830-8. **[SCI-E]**

11. Analysis of Design Parameters in Safety-Critical Computers, by H. Ahangari, F. Atik, Y. I. Ozkok, A. Yildirim, S. O. Ata and O. Ozturk. IEEE Transactions on Emerging Topics in Computing, July-Sept. 2020, pp. 712-723, Vol. 8. DOI: 10.1109/TETC.2018.2801463. **[SCI-E]**

12. Adaptive Thread Scheduling in Chip Multiprocessors, by Ismail Akturk and Ozcan Ozturk. International Journal of Parallel Programming, Volume 47, 1014-1044, 2019. DOI: 10.1007/s10766-019-00637-y. **[SCI-E]**

13. A Novel Heterogeneous Approximate Multiplier for Low Power and High Performance, Ihsen Alouani, Hamzeh Ahangari, Ozcan Ozturk, Smaïl Niar, IEEE Embedded Systems Letters 10(2): 45-48, 2018. **[SCI-E]**

14. Classifying Data Blocks at Subpage Granularity with an On-Chip Page Table to Improve Coherence in Tiled CMPs, by M. Soltaniyeh, I. Kadayif, and O. Ozturk. IEEE Trans. on CAD of Integrated Circuits and Systems 37(4): 806-819, 2018. **[SCI]**

15. A Template-Based Design Methodology for Graph-Parallel Hardware Accelerators, by Andrey Ayupov, Serif Yesil, Muhammet Mustafa Ozdal, Taemin Kim, Steven M. Burns, Ozcan Ozturk. IEEE Transactions on CAD of Integrated Circuits and Systems 37(2): 420-430, 2018. **[SCI]**

16. Graph Analytics Accelerators for Cognitive Systems, by Muhammet Mustafa Ozdal, Serif Yesil, Taemin Kim, Andrey Ayupov, John Greth, Steven Burns, and Ozcan Ozturk, IEEE MICRO, Volume: 37, Issue: 1, Pages: 42 - 51, DOI:

10.1109/MM.2017.7, 2017. **[SCI]**

17. Optimization-Based Power and Thermal Management for Dark Silicon Aware 3D Chip Multiprocessors Using Heterogeneous Cache Hierarchy, by A. Asad, M. Fathy, M. R. J. Motlagh, O. Ozturk, Microprocessors and Microsystems (MICPRO) - Embedded Hardware Design, Volume 51, Pages 76-98, 2017. **[SCI-E]**
18. Cache Hierarchy-Aware Query Mapping On Emerging Multicore Architectures, by Ozcan Ozturk, Umut Orhan, Wei Ding, Praveen Yedlapalli, Mahmut Kandemir, IEEE Transactions on Computers (TC), 66(3): 403-415 (2017). **[SCI]**
19. Pipelined Fission for Stream Programs with Dynamic Selectivity and Partitioned State, Bugra Gedik, Habibe G Özsema, Ozcan Ozturk, Journal of Parallel and Distributed Computing, 96: 106-120, 2016. **[SCI]**
20. Fault-Tolerant Topology Generation Method for Application-Specific Network-on-Chips, by Tosun, S.; Ajabshir, V.; Mercanoglu, O.; Ozturk, O. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 34, no. 9, pp. 1495-1508, Sept. 2015. **[SCI]**
21. Application mapping algorithms for mesh-based network-on-chip architectures, by Suleyman Tosun, Ozcan Ozturk, Erencan Ozkan and Meltem Ozen, The Journal of Supercomputing, Volume 71, Issue 3, Pages 995-1017, 2015. **[SCI]**
22. Energy Reduction in 3D NoCs Through Communication Optimization, O. Ozturk, I. Akturk, I. Kadayif, and S. Tosun, Computing, Vol 97, Issue 6, Pages 593-609, 2015 **[SCI]**
23. Voltage Island Based Heterogeneous NoC Design Through Constraint Programming, by Ayhan Demiriz, Nader Bagherzadeh, Ozcan Ozturk. Computers and Electrical Engineering, Computers & Electrical Engineering, Volume 40, Issue 8, Pages 307-316, 2014. **[SCI-E]**
24. Application-Specific Heterogeneous Network-on-Chip Design, by Dilek Demirbas; Ismail Akturk; Ozcan Ozturk; Ugur Gudukbay. The Computer Journal, Volume 57, Issue 8, pages 1117-1132, August 2014. [**SCI-E]**
25. Improving Application Behavior on Heterogeneous Manycore Systems Through Kernel Mapping, by O. Erdil Albayrak, Ismail Akturk, and Ozcan Ozturk, Parallel Computing, Volume 39, Issue 12, December 2013, Pages 867-878. **[SCI]**
26. A Decoupled Local-Memory Allocator, by B. Diouf, C. Hantas, A. Cohen, O. Ozturk, and J. Palsberg, ACM Transactions on Architecture and Code Optimization (TACO), Vol. 9, No. 4, Article 34, Publication date: January 2013. **[SCI-E]**
27. Compiler-Directed Energy Reduction Using Dynamic Voltage Scaling and Voltage Islands for Embedded Systems, by O. Ozturk, M. Kandemir, and G. Chen, IEEE Transactions on Computers (TC), Vol. 62, No. 2, pages 268-278, February 2013. **[SCI]**
28. Hardware/Software Approaches for Reducing the Process Variation Impact on Instruction Fetches, by I. Kadayif, M. Turkcan, S. Kiziltepe, and O. Ozturk, ACM Transactions on Design Automation of Electronic Systems (TODAES), Volume 18, Number 4, Pages 54:1-54:23, October 2013. [**SCI-E]**
29. Reliability-Aware Heterogeneous 3D Chip Multiprocessor Design, by Ismail Akturk and Ozcan Ozturk. Journal of Electronic Testing Theory and Applications, Volume 29, Issue 2, pages 177-184, April 2013. [**SCI-E]**
30. Reducing Memory Space Consumption Through Dataflow Analysis, by O. Ozturk, Computer Languages, Systems & Structures, Volume 37, Issue 4, October 2011, pages 168-177. **[SCI-E]**
31. Multicore Education Through Simulation, by O. Ozturk, IEEE Transactions on Education (TE), Volume 54, Issue 2, pages 203-209, May 2011. **[SCI]**
32. Data Locality and Parallelism Optimization Using A Constraint-Based Approach, by O. Ozturk, Journal of Parallel and Distributed Computing (JPDC), volume 71, issue 2, pages 280-287, 2011. **[SCI]**
33. Heterogeneous NoC Design Through Evolutionary Computing, by Ozcan Ozturk and Dilek Demirbas, International Journal of Electronics, Francis & Taylor, Volume 97, No. 10, pages 1139–1161, 2010. **[SCI]**
34. On-Chip Memory Space Partitioning for Chip Multiprocessors using Polyhedral Algebra, by O. Ozturk, M. Kandemir, M. J. Irwin. IET Computers & Digital Techniques, Volume 4, Issue 6, pages 484-498, 2010. **[SCI-E]**
35. Improving Chip Multiprocessor Reliability Through Code Replication, by Ozcan Ozturk. Computers & Electrical Engineering, Elsevier, Issue 36, pages 480–490, 2010. **[SCI-E]**
36. Compiler Directed Communication Reliability Enhancement for Chip Multiprocessors, by O. Ozturk, M. Kandemir, S. Narayanan, and M. J. Irwin. ACM SIGPLAN Notices, Vol. 45, No. 4, pp. 85-94, 2010. **[SCI-E]**
37. Using Data Compression for Increasing Memory System Utilization, by Ozcan Ozturk, Mahmut Kandemir, Mary J. Irwin. IEEE Transactions on Computer Aided Design, Volume 28, Number 6, pages 901-914, June 2009. **[SCI]**
38. Shared scratch pad memory space management across applications, by O. Ozturk, M. Kandemir, S. W. Son, and I. Kolcu. International Journal of Embedded Systems, Vol. 4, No.1 pp. 54 – 65, 2009.
39. ILP Based Energy Minimization Techniques for Banked Memories, by O. Ozturk and M. Kandemir. ACM Transactions on Design Automation of Electronic Systems (TODAES), Volume 13 , Issue 3, July 2008. **[SCI-E]**
40. Access Pattern-Based Code Compression For Memory-Constrained Systems, by O. Ozturk, M. Kandemir, and G. Chen. ACM Transactions on Design Automation of Electronic Systems (TODAES), Vol. 13, Issue 4, September 2008. **[SCI-E]**
41. Compiler-Directed Energy Optimization for Parallel Disk Based Systems, by S. W. Son, G. Chen, O. Ozturk, M. Kandemir, and A. Choudhary, IEEE Transactions on Parallel and Distributed Systems (TPDS), Volume 18, Number 9, pp. 1241-1257, September, 2007. **[SCI]**
42. Optimizing Array-Intensive Applications for On-Chip Multiprocessors, by I.Kadayif, M.Kandemir, G.Chen, O.Ozturk, M.Karakoy, and U.Sezer. IEEE Transactions on Parallel and Distributed Systems (TPDS), Volume 16, Number 5, May 2005. **[SCI]**
43. An ILP formulation for task scheduling on heterogeneous chip multiprocessors, by S. Tosun, N. Mansouri, and M. Kandemir. Lecture Notes in Computer Science (LNCS) 4263 Springer 2006, ISBN 3-540-47242-8.
44. An ILP-Based Approach to Locality Optimization, by G. Chen, O. Ozturk, and M. Kandemir. Lecture Notes in Computer Science (LNCS) 3602 Springer 2004, Languages and Compilers for High Performance Computing, pages 149-163.

45. Using data compression to increase energy savings in multi-bank memories, by M.Kandemir, O.Ozturk, M.J.Irwin, and I.Kolcu. Lecture Notes in Computer Science (LNCS) 3149 Springer 2004, ISBN 3-540-22924-8, pages 310-317.

Conferences:

1. Compiler-Supported Selective Software Fault Tolerance, by Tuncer Turhan, Hakan Tekgul, and Ozcan Ozturk. In the Proceedngs of IEEE Conference on Dependable and Secure Computing (DSC'23), Tampa, FL USA, 7 – 9 November, 2023.
2. Fast Compiler Optimization Flag Selection, by Melih Peker and Ozcan Ozturk. In the Proceedings of the 34th International Workshop on Rapid System Prototyping (RSP'23), Embedded Systems Week (ESWEEK), September 17-22, 2023, Hamburg, Germany.
3. Utilizing Prefetch Buffers for Iterative Graph Applications, by Burak Ocalan and Ozcan Ozturk. In the Proceedings of the 26th Euromicro Conference on Digital System Design (DSD), Durres, Albania, September 6-8, 2023.
4. Automatic Selection of Compiler Optimizations by Machine Learning, by Melih Peker, Özcan Özturk, Süleyman Yildirim, and Mahiye Uluyagmur Öztürk. In the Proceedings of the 31. IEEE Signal Processing and Communications Applications Conference (SIU'23), Istanbul, 5-8 July 2023.
5. Teaching Parallel Computing: Architectures, Algorithms, and Applications, by Ozcan Ozturk. In the Proceedings of the EduPar 2023, May 15, 2023, St. Petersburg, FL, USA.
6. Coherency Traffic Reduction in Manycore Systems, by Erdem Derebasoglu, Ismail Kadayif, and Ozcan Ozturk. In the Proceedings of the 25th Euromicro Conference on Digital System Design (DSD), Maspalomas, Gran Canaria, Spain, Aug. 31th – September 2nd, 2022.
7. RISC-V Instruction Set Extension for Graph Applications, by Mehmetali Semi Yenimol, Gülce Pulat, and Ozcan Ozturk. In the Proceedings of the Sixth Workshop on Computer Architecture Research with RISC-V (CARRV 2022), June 2022, co-located with ISCA 2022.
8. Çizge Uygulamalarına Özel İşlemci Tasarımı, by Gulce Pulat, Aamir Saeed, Mehmetali Semi Yenimol, Utku Gulgec, and Ozcan Ozturk. In the Proceedings of the 30. IEEE Signal Processing and Communications Applications Conference (SIU'22), Safranbolu, Karabuk, 15-18 May 2022.
9. GateKeeper-GPU: Accelerated Pre-Alignment Filtering in Short Read Mapping, Zülal Bingöl, Mohammed Alser, Ozcan Ozturk, Can Alkan. 20th IEEE International Workshop on High Performance Computational Biology (HiCOMB) 2021, May 17, 2021. Portland, Oregon, USA.
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PRESENTATIONS

1. Compiler-Supported Selective Software Fault Tolerance, IEEE Conference on Dependable and Secure Computing (DSC'23), Tampa, FL USA, 7 – 9 November, 2023.

2. Heterogeneous Computing and Domain Specific Architectures. Bilkent University, Ankara. October, 2022.

3. Fast Compiler Optimization Flag Selection, The 34th International Workshop on Rapid System Prototyping (RSP'23), Embedded Systems Week (ESWEEK), September 17-22, 2023, Hamburg, Germany.

4. Utilizing Prefetch Buffers for Iterative Graph Applications, The 26th Euromicro Conference on Digital System Design (DSD), Durres, Albania, September 6-8, 2023.

5. Automatic Selection of Compiler Optimizations by Machine Learning, The 31. IEEE Signal Processing and Communications Applications Conference (SIU'23), Istanbul, 5-8 July 2023.

6. Teaching Parallel Computing: Architectures, Algorithms, and Applications. EduPar 2023, May 15, 2023, St. Petersburg, FL, USA.

7. Heterogeneous Computing and Domain Specific Architectures. Bilkent University, Ankara. October, 2022.

8. RISC-V Instruction Set Extension for Graph Applications, The Sixth Workshop on Computer Architecture Research with RISC-V (CARRV 2022), June 2022, co-located with ISCA 2022.

9. Coherency Traffic Reduction in Manycore Systems, The 25th Euromicro Conference on Digital System Design (DSD), Maspalomas, Gran Canaria, Spain, Aug. 31th – Sept. 2nd, 2022.

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11. Heterogeneous Computing and Domain Specific Architectures, by Ozcan Ozturk. University of Hauts de France, Valenciennes, France. December, 2021.

12. Instruction-level Reliability Improvement for Embedded Systems, by Hakan Tekgul and Ozcan Ozturk. DTS 2020 - IEEE Design and Test Symposium, June 7-10, 2020, Hammamet, Tunus. . **(Best Paper Award)**

13. Hierarchical Collborative Platform for Autonomous Driving, by Hamza Ouarnoughi, Mohamed Ayoub Neggaz, Ege Berkay Gulcan, Ozcan Ozturk and Smail Niar. INTESA Workshop 2019 - INTelligent Embedded Systems Architectures and Applications, co-located with ESWEEK 2019, Oct 13 - 18, 2019, NYU Center for Cyber-Security, New York, USA.

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16. Message From the General Chair, O. Ozturk. In Proc. of 2017 IEEE International Conference on Microelectronic Systems Education (MSE), Lake Louise, AB, Canada, May 11-12, 2017.

17. Analysis of Design Parameters in SIL-4 Safety-Critical Computer, by H. Ahangari, Y. OZKOK, A. Yildirim, F. SAY, F. Atik, and O. Ozturk. (2017). 10.1109/RAM.2017.7889787. In Pro. of IEEE 2017 Annual Reliability and Maintainability Symposium (RAMS), Orlando, FL, January 2017.

18. Keynote 1: "Analysis of design parameters in safety-critical systems", International Design and Test (IDT) Symposium, Hammamet, Tunus, December 2016.

19. AutopaR: An Automatic Parallelization Tool for Recursive Calls, The Fifth International Workshop on Parallel Software Tools and Tool Infrastructures (PSTI 2014), Minneapolis, MN, September, 2014.

20. Adaptive Compute-phase Prediction and Thread Prioritization to Mitigate Memory Access Latency, International Workshop on Manycore Embedded Systems, June 2014, Minneapolis, MN.

21. Staggered Latch Bus: A Reliable Offset Switched Architecture for Long On-Chip Interconnect, 21st IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC), Istanbul, Turkey, October 2013.

22. Effective Kernel Mapping for OpenCL Applications in Heterogeneous Platforms,
International Conference on Parallel Processing, Pittsburgh, PA, USA, September 2012.

23. Reliability-Aware 3D Chip Multiprocessor Design,
Manufacturable and Dependable Multicore Architectures at Nanoscale (MEDIAN'12), Annecy, France, June 2012.

24. Manycore Processors and Parallel Programming,
Invited Speaker, National High Performance Computing Conference, Ankara, Nisan 2012.

25. Optimizing Parallel Behavior of OpenFOAM,
Stanford University, Stanford, CA, May 2011.

26. Cache-Aware Application and Thread Scheduling,
NEC Labs, Princeton, NJ, June 2011.
27. Multicore Education Through Simulation,
Microelectronic Systems Education (MSE'09), San Francisco, CA, July 2009.
28. Compiler Optimizations for Chip Multiprocessors,
Munich, Germany, May 2009, HiPEAC (European Network of Excellence on High Performance and Embedded Architecture and Compilation)
29. Compiler-Guided Optimizations for Memory-Constrained Embedded Systems,
Koç Üniversity, Istanbul, April 2007.
30. Memory Hierarchy Design For Chip Multiprocessors - A Compiler Directed Approach,
Bilkent Üniversiy, April 2007.
31. Enhancing Locality In Two-Dimensional Space Through Integrated Computation And Data Mappings
VLSI Design Conference 2007, Bangalore, India, January 2007.
32. A Process Scheduler-Based Approach to NoC Power Management
VLSI Design Conference 2007, Bangalore, India, January 2007.
33. Locality-Aware Distributed Loop Scheduling For Chip Multiprocessors
VLSI Design Conference 2007, Bangalore, India, January 2007.
34. Cache miss clustering for banked memory systems
VLSI Design Conference 2007, Bangalore, India, January 2007.
35. Cache miss clustering for banked memory systems
ICCAD 2006, San Jose, CA, November 2006.
36. Multi-level On-chip Memory Hierarchy Design for Embedded Chip Multiprocessors
ICPADS 2006, Minneapolis, MN, June 2006.
37. Selective Code/Data Migration for Reducing Communication Energy in Embedded MpSoC Architectures
38. An ILP Based Approach to Address Code Generation for Digital Signal Processors
GLSVLSI 2006, Philadelphia, PA, April 2006.
39. Managing SPM Space Based on Inter-Application Data Sharing
ODES-4, Manhattan, New York, March 2006.
40. Dynamic Scratch-Pad Memory Management for Irregular Array Access Patterns
DATE 2006, Munich, Germany, March 2006.
41. Dynamic Partitioning of Processing and Memory Resources in Embedded MPSoC Architectures
DATE 2006, Munich, Germany, March 2006.
42. M-Opt: Memory Design Optimizer tool demonstration
GSRC Quarterly Workshop, Berkeley, CA, March 2006.
43. Shared Scratch-Pad Memory Space Management
ISQED 2006, San Jose,CA, March 2006.
44. An Integer Linear Programming Based Approach to Simultaneous Memory Space Partitioning and Data Allocation for Chip Multiprocessors
ISVLSI 2006, Karlsruhe, Germany, March 2006.
45. Task Recomputation in Memory Constrained Embedded Multi-CPU Systems
ISVLSI 2006, Karlsruhe, Germany, March 2006.
46. Leakage-Aware SPM Management
ISVLSI 2006, Karlsruhe, Germany, March 2006.
47. On-Chip Memory Management for Embedded MpSoC Architectures Based on Data Compression
SOCC 2005, Washington, DC, September 2005.
48. Workload Clustering for Increasing Energy Savings on Embedded MPSoCs
SOCC 2005, Washington, DC, September 2005.
49. Automatic Memory Partitioning*:*
GSRC Quarterly Workshop, Anaheim, CA, June 2005
50. Exploiting Inter-Processor Data Sharing for Improving Behavior of Multi-Processor SoCs*:*
ISVLSI 2005, Tampa, Florida, May 2005
51. Access Pattern-Based Code Compression for Memory-Constrained Embedded Systems
DATE 2005, Munich, Germany, March 2005.
52. BB-GC: Basic-Block Level Garbage Collection
DATE 2005, Munich, Germany, March 2005.
53. Nonuniform Banking for Reducing Memory Energy Consumption
DATE 2005, Munich, Germany, March 2005.
54. Increasing Register File Immunity to Transient Errors
DATE 2005, Munich, Germany, March 2005.
55. Reliability-Centric High-Level Synthesis
DATE 2005, Munich, Germany, March 2005.
56. Dynamic On-Chip Memory Management for Chip Multiprocessors
CASES 2004, Washington D.C., September 2004